METHOD TO INCREASE HEAD VOLTAGE SWING AND TO REDUCE THE RISE TIME OF WRITE DRIVER

FIELD OF THE INVENTION

The present invention is generally related to the field of mass media information storage devices, and more particularly to a voltage-mode boosting circuit to increase head voltage swing while reducing the rise time of a write driver current switch driving a thin film transducer.

BACKGROUND OF THE INVENTION

Hard disk drives are mass storage devices that include a magnetic storage media, e.g. rotating disks or platters, a spindle motor, read/write heads, an actuator, a pre-amplifier, a read channel, a write channel, a servo circuit, and control circuitry to control the operation of hard disk drive and to properly interface the hard disk drive to a host system or bus. Figure 1 shows an example of a prior art disk drive mass storage system 10. Disk drive system 10 interfaces with and exchanges data with a host 32 during read and write operations. Disk drive system 10 includes a number of rotating platters 12 mounted on a base 14. The platters 12 are used to store data that is represented as magnetic transitions on the magnetic platters, with each platter 12 coupleable to a head 16 which transfers data to and from a preamplifier 26. The preamp 26 is coupled to a synchronously sampled data (SSD) channel 28 comprising a read channel and a write channel, and a control circuit 30. SSD channel 28 and control circuit 30 are used to

process data being read from and written to platters 12, and to control the various operations of disk drive mass storage system 10. Host 32 exchanges digital data with control circuit 30.

Data is stored and retrieved from each side of the magnetic platters 12 by heads 16 which comprise a read head 18 and a write head 20 at the tip thereof. The conventional readhead 18 and writehead 20 comprise magneto-resistive heads adapted to read or write data from/to platters 12 when current is passed through them. Heads 16 are coupled to preamplifier 26 that serves as an interface between read/write heads 18/20 of disk/head assembly 10 and SSD channel 28. The preamp 26 provides amplification to the waveform data signals as needed. A preamp 26 may comprise a single chip containing a reader amplifier 27, a writer amplifier, fault detection circuitry, and a serial port, for example. Alternatively, the preamp 26 may comprise separate components rather than residing on a single chip.

In the preamplifier 26, the voltage at the output of the write driver circuit driving a thin film head via an external flex cable interconnection is limited by many constraints, such as supply voltages, head room in the circuitry, and the impedance of the external connection. If the write driver's output head voltage swing is increased, more voltage is delivered to the thin film head to saturate the media faster, which in turn allows the data to be written at a higher data rate.

There is a need for an improved voltage-mode write driver circuit that increases the write driver's output head voltage swing to achieve higher write data rates.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages as a voltage-mode boosting write driver circuit including two sets of PMOS transistors, one set for voltage boosting each half of a high current H-switch driving a thin film head. One set of PMOS transistor includes one transistors which turns on hard to pull output pin HY up very fast towards Vcc, while the other transistor pulls up the base of one of the H-switch transistors to in turn pull down hard the output pin HX toward VEE. The simultaneous actions of pulling output pin HY up and output pin HX down quickly produces a larger differential voltage swing across the output HX and HY, resulting in faster slew rate of the write current output. Likewise, the other set of PMOS transistors associated with the other half of the H-switch are likewise coupled to the other half of the H-switch to pull down pin HY and pull up pin HX. Regardless of whether the differential input signal is positive or negative, the voltage differential across the output pins HX and HY always has a large differential voltage swing and a fast slew rate. Also, by using existing transient currents of the pre-driver to drive the PMOS devices, lower power dissipation and smaller number of devices used are achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a conventional disk drive system including multiple rotating disks or platters, read/write heads, a piezo actuator, a servo circuit, and associated amplifier and control circuitry;

Figure 2 depicts a voltage-mode boosting write driver circuit according to the present invention including two sets of PMOS transistors each coupled to the high-current H-switch and adapted to each pull high one output pin while

simultaneously pulling low the other output pin to achieve a larger differential voltage swing;

Figure 3 is a waveform diagram illustrating the increased differential voltage swing across outputs pins HX and HY, and also resulting in a faster slew rate; and

Figure 4 illustrates both the increased voltage swing and a quicker settling of the drive signal achieved to the impedance matching of the H-switch to the thin film head and respective interconnection.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 2 depicts a voltage-mode boosting write driver circuit 40 according to a preferred embodiment of the present invention. Circuit 40 of Figure 2 achieves technical advantages by increasing the maximum head voltage swing while also reducing the rise time of the write driver current to driving a thin film head L0. The inputs of circuit 40 are the write data VECL and VECL_N pin. They are differential voltage signals with an ECL level swing of 200-300 mV differential. The differential outputs of circuit 40 are HX and HY, which drive the flex interconnection T0, connected to the thin film transducer L0. The typical values for a high end system (>1Gb/s) of T0 and L0 are: Interconnection's differential input impedance of 64 Ohms and transmission delay of 250 psec, the thin film inductance of 7 nH. The typical supply voltages are: Vcc=+5V +/-10%, Vee=-5V +/-5% and ground.

The main H-switch 42 switches the write current Iw and is composed of

an upper pair of bipolar transistors Q6 and Q7, and a lower pair of bipolar transistors Q2 and Q3. Advantageously, resistors R3 and R4 are impedance-matched resistors and which together match the differential impedance of the interconnection T0. In the steady state, the differential output impedance of the write driver circuit 40 is 64 Ohms, which is matched to the interconnection T0 impedance being 64 Ohms. With no signal reflection occurring due to the matched impedances, the write current Iw settles quickly with minimum ringing to achieve high data rate, as shown in Figure 4.

Operation

Assume the input VECL signal is high and input VECL_N signal is low with a differential logic level of 300mV. Transistors Q8 and Q0-Q2 are on, and transistors Q10 and Q3-Q5 are off. The base of transistor Q6 is pulled down lower than the base of transistor Q7. Accordingly, most of the write current Iw will flow from the transistor Q2 collector, through the pin HX to the interconnection T0, and to the thin film head L0. The return current path is through resistor R4 and transistor Q7. Transistor Q6 is still on due to current provided by transistor Q1 which ensures that the resistors R3+R4=64 Ohms impedance matches the interconnection's impedance.

According to the present invention, when the input voltage signal switches from low to high, transistor Q8 produces a very high transient current of 50-60mA in a very short period of time. This produced transient current responsively pulls down both the gates of the PMOS transistors M0 and M1, collectively shown at 44, and turns them on very hard. PMOS transistor M1 turning on hard responsively pulls the output pin HY up very fast toward Vcc, while PMOS transistor M0 pulls up the bases of transistor Q0-Q2 and thus responsively pulls

output pin HX down hard toward Vee. The simultaneous actions of quickly pulling pin HY up and pin HX down produces a larger differential voltage swing output at HX and HY, as shown in Figure 3. The result is faster slew rate of the write current output.

Likewise, the second pair 46 of PMOS transistors M2 and M3 are coupled to the right half of the H-switch 42. When the input voltage signal switches from high to low, transistor Q10 produces a very high transient current of 50-60mA in a very short period of time. This produced transient current responsively pulls down both the gates of the PMOS transistors M2 and M3, collectively shown at 46, and turns them on very hard. PMOS transistor M2 turning on hard responsively pulls the output pin HX up very fast toward Vcc, while the PMOS transistor M3 pulls up the bases of transistor Q3-Q5 and thus pulls down the output HY hard toward Vee. The simultaneous action of quickly pulling pin HX up and pin HY down produces a larger differential voltage swing across the outputs HX and HY, as shown at 52 in Figure 3, as opposed to the differential swing 50 without the PMOS boosting transistors 44 and 46.

As depicted in Figure 2, the additional pairs of boosting PMOS transistors 44 and 46 significantly increase the voltage swing across the output pins HX and HY, wherein the voltage swing is shown at 50 without the use of the sets of PMOS transistors 44 and 46, and depicted at 52 when including the sets of boosting PMOS transistors 44 and 46. In the case when Vcc is +5 volts, and Vee is -5 volts, there is seen in Figure 3 an increase voltage swing of approximately 0.9 volts, which is roughly a 15% increase in the differential voltage swing, which is very significant. This additional voltage swing also has an increased slew rate of the output voltage signal, as also depicted in Figure 3, due to the impedance matching of the H-circuit 42 to the interconnection T0 and head L0.

Figure 4 further depicts that the write current Iw settles quickly and with minimum ringing due to the impedance matching of the H-switch resistors R3 and R4 to the impedance of the flex cable interconnection, thereby achieving a higher write data rate.

Though the invention has been described with respect to a specific preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.